

Notice of References Cited	Application/Control No. 09/976,286		Applicant(s)/Patent Under Reexamination MERIBOUT, MAHMOUD	
	Examiner Mary J. Steelman		Art Unit 2122	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,966,534	10-1999	Cooke et al.	717/155
*	B	US-6,075,935	06-2000	Ussery et al.	716/17
*	C	US-6,192,504 B1	02-2001	Pfluger et al.	716/1
*	D	US-6,233,540 B1	05-2001	Schaumont et al.	703/14
*	E	US-6,330,530 B1	12-2001	Horiguchi et al.	704/4
*	F	US-6,708,325 B2	03-2004	Cooke et al.	717/124
*	G	US-2002/0099756 A1	07-2002	Catthoor et al.	709/102
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Akturan, Cagdas; Jacome, Margarida F; "RS-FDRA: A Register Sensitive Software Pipelining Algorithm for Embedded VLIW Processors", p. 67-72, ACM April 2001, retrieved from IEEE 08/16/2004.			
	V	Dick, Robert; Jha, Niraj K; "MOGAC: A Multiobjective Genetic Algorithm for Hardware-Software Cosynthesis of Distributed Embedded Systems", p. 920-935, 1998 IEEE, retrieved 08/16/2004.			
	W	Lucke, Lori E; Parhi, Keshab K; "Generalized ILP Scheduling and Allocation for High-Level DSP Synthesis", p. 541-544, IEEE 1993, retrieved 08/16/2004.			
	X	Johannes, Frank M; "Partitioning of VLSI Circuits and Systems", 1996 ACM, retrieved 08/16/2004.			

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.